H

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/967,220	09/28/2001	Dong-Yuan Chen	42390P11197	7151

7590 04/07/2004

Blakely, Sokoloff, Taylor & Zafman
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1030

EXAMINER	
YIGDALL, MICHAEL J	
ART UNIT	**PAPER NUMBER**
2122	

DATE MAILED: 04/07/2004

h

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/967,220	Applicant(s) CHEN ET AL.	
	Examiner Michael J. Yigdall	Art Unit 2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 28 September 2001.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-30 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 28 September 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are pending and have been examined. The priority date considered for the application is 28 June 2001.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 6, 7, 10-14, 16, 17, 20-22 and 24-26 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pat. No. 6,134,710 to Levine et al. (hereinafter Levine).

With respect to claim 1, Levine discloses a method comprising:

(a) selecting one or more microarchitecture events relating to a microprocessor executing an application process to be monitored by one or more hardware monitors (see column 2, lines 8-14, which shows selecting events to be recorded by hardware performance monitor counters);

(b) establishing parameters regarding the monitoring of the microarchitecture events by setting one or more monitor control vectors (see column 2, lines 12-20, which shows setting monitor control registers, i.e. control vectors, to establish monitoring parameters);

(c) processing profile data captured by the one or more hardware monitors regarding the occurrence of the one or more microarchitecture events (see column 11, lines 24-34, which shows processing the profile data to generate effective address tables);

(d) identifying a region of interest in the application process for optimization based at least in part on the captured profile data (see column 12, lines 1-6, which shows analyzing the tables based on the profile data to identify a location or region for optimization); and

(e) optimizing the region of interest in the application process (see column 13, lines 63 to column 14, line 4, which shows applying the optimizations to the application process).

With respect to claim 2, Levine further discloses the limitation wherein setting each monitor control vector comprises setting one or more fields of the monitor control vector to control the monitoring of the microarchitecture event (see column 2, lines 8-20, which shows setting fields in the control registers to control the event counting or monitoring).

With respect to claim 3, Levine further discloses the limitation wherein setting the one or more fields of each monitor control vector includes setting a control field to establish the type of microarchitecture event that is monitored by a hardware monitor (see column 8, lines 44-52, which shows setting control fields to select the types of events to be monitored).

With respect to claim 4, Levine further discloses the limitation wherein setting the one or more fields of each monitor control vector includes setting a trigger field to control when a microarchitecture event is monitored (see column 8, lines 23-24 and 35-39, which show setting trigger fields to control when events are counted or monitored).

With respect to claim 6, Levine further discloses obtaining the captured profile data for each monitored microarchitecture event from a profile buffer (see column 11, lines 42-53, which shows obtaining the profile data from a buffer).

With respect to claim 7, Levine further discloses the limitation wherein obtaining the captured profile data for a microarchitecture event from the memory buffer occurs when a memory buffer in the profile buffer that is assigned for the monitored microarchitecture event is fully allocated (see column 11, lines 42-53, which shows that the buffer is of a predetermined size and is used in a round-robin fashion, and is therefore fully allocated when the profile data is obtained before being overwritten).

With respect to claim 10, Levine further discloses the limitation wherein the microarchitecture event monitored is an instruction cache miss event (see column 10, lines 2-8, which shows instruction cache miss events, and column 10, lines 15-19 and 34-36, which show counting or monitoring such cache misses).

With respect to claim 11, see the reasoning set forth above for claim 1. The operations recited by claim 11 are analogous to the method steps recited by claim 1. Note that Levine further discloses a machine-readable medium having stored thereon data representing instructions that, when executed by a processor, cause the processor to perform the recited operations (see column 1, line 65 to column 2, line 1, and column 2, lines 28-44).

With respect to claim 12, see the reasoning set forth above for claim 2. The operations recited by claim 12 are analogous to the method steps recited by claim 2.

With respect to claim 13, see the reasoning set forth above for claim 3. The operations recited by claim 13 are analogous to the method steps recited by claim 3.

With respect to claim 14, see the reasoning set forth above for claim 4. The operations recited by claim 14 are analogous to the method steps recited by claim 4.

With respect to claim 16, see the reasoning set forth above for claim 6. The operations recited by claim 16 are analogous to the method steps recited by claim 6.

With respect to claim 17, see the reasoning set forth above for claim 7. The operations recited by claim 17 are analogous to the method steps recited by claim 7.

With respect to claim 20, see the reasoning set forth above for claim 10. The operations recited by claim 20 are analogous to the method steps recited by claim 10.

With respect to claim 21, Levine discloses a hardware assisted dynamic optimizer (see the abstract and FIG. 2), comprising:

(a) an interface to a microprocessor through which the hardware assisted dynamic optimizer establishes parameters regarding the monitoring of one or more microarchitecture events occurring during the execution of an application by the microprocessor (see column 2, lines 8-20, which shows setting addressable monitor control registers to select events to be recorded and establish monitoring parameters);

(b) one or more handler routines, each handler routine including instructions to process profiles of a monitored microarchitecture event that are captured by the microprocessor (see

column 10, line 67 to column 11, line 5, which shows a handler routine for processing captured profile data, and column 11, lines 24-34, which shows processing the data to generate effective address tables); and

(c) one or more optimizers, each optimizer including instructions for optimizing a section of the application, the section of the application being chosen by the hardware assisted dynamic optimizer at least in part based on the captured profiles of a monitored microarchitecture event (see column 12, lines 1-6, which shows analyzing the tables based on the profile data to identify a location or region for optimization, and column 13, line 63 to column 14, line 4, which shows applying the optimizations to the application).

With respect to claim 22, Levine further discloses the limitation wherein each monitor control vector includes a plurality of fields to control the monitoring of the microarchitecture event, the plurality of fields being set by the hardware assisted dynamic optimizer (see column 2, lines 8-20, which shows setting fields in the control registers to control the event counting or monitoring).

With respect to claim 24, Levine further discloses the limitation wherein optimizing a section of the application includes increasing the speed of processing of the section of the application (see column 1, lines 19-23, which shows that delays in executing an application may be caused by long table walks or long cache misses; see also column 1, lines 58-62, which shows that the optimizations minimize the effects of such table walks and cache misses, i.e. increase the speed of processing the application).

With respect to claim 25, Levine further discloses the limitation wherein the hardware assisted dynamic optimizer obtains the captured profiles of the one or more microarchitecture events from a profile buffer (see column 11, lines 42-53, which shows obtaining the profile data from a buffer).

With respect to claim 26, Levine further discloses the limitation wherein at least a portion of the profile buffer is architecturally visible to the hardware assisted dynamic optimizer (see column 11, lines 42-53, which shows accessing the buffer, which means the buffer is architecturally visible to the optimizer).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5, 15, 23 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levine, as applied to claims 2, 12, 22 and 26 above, respectively.

With respect to claim 5, Levine discloses setting an interrupt field to cause a handler routine to process the profile data when an event occurs (see column 8, lines 24-35, which shows the interrupt field in the control register, and column 10, line 67 to column 11, line 5, which shows the handler routine).

Levine does not expressly disclose the limitation wherein setting the one or more fields of each monitor control vector includes storing a pointer in a handler field, the pointer identifying a handler routine to process the captured profile data associated with the occurrence of a microarchitecture event corresponding to the monitor control vector.

However, a pointer is inherently used in the Levine system to identify the handler routine. The address of the routine must be known in order to invoke the routine and process the captured profile data. It is also well known in the art that a pointer may be stored, for example, in a field of a control vector or register.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to store the pointer to the handler routine of Levine in a field of the control registers taught by Levine, for the purpose of identifying the address of the routine.

With respect to claim 15, see the reasoning set forth above for claim 5. The operations recited by claim 15 are analogous to the method steps recited by claim 5.

With respect to claim 23, Levine further discloses the limitation wherein the plurality of fields includes a control field to establish the type of microarchitecture event that is monitored (see column 8, lines 44-52, which shows setting control fields to select the types of events to be monitored) and a trigger field to control when the microarchitecture event is monitored (see column 8, lines 23-24 and 35-39, which show setting trigger fields to control when events are counted or monitored).

Although Levine discloses setting an interrupt field to cause a handler routine to process the profile data when an event occurs (see column 8, lines 24-35, which shows the interrupt field

in the control register, and column 10, line 67 to column 11, line 5, which shows the handler routine), Levine does not expressly disclose the limitation wherein the plurality of fields includes a handler field to store a pointer to the handler routine for the microarchitecture event.

However, a pointer is inherently used in the Levine system to identify the handler routine. The address of the routine must be known in order to invoke the routine and process the captured profile data. It is also well known in the art that a pointer may be stored, for example, in a field of a control vector or register.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to store the pointer to the handler routine of Levine in a field of the control registers taught by Levine, for the purpose of identifying the address of the routine.

With respect to claim 27, although Levine discloses a buffer for profile data (see column 11, lines 42-53), Levine does not expressly disclose the limitation wherein the profile buffer has a first level and a second level, and wherein the hardware assisted dynamic optimizer sets conditions for transferring captured profiles from the first level to the second level.

However, Levine discloses a memory hierarchy having two cache levels, in order balance cost and performance (see column 6, line 61 to column 7, line 8, which shows that the first level is faster but more costly than the second level). It is well known in the art that data is transferred between the cache levels in such memory hierarchies.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the buffer of Levine with two levels, and to transfer profile data from the first level to the second level given one or more set conditions, for the purpose of creating a hierarchy that balances cost and performance.

6. Claims 8, 9, 18, 19 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levine, as applied to claims 7, 17 and 27 above, respectively, in view of U.S. Pat. No. 6,622,300 to Krishnaswamy et al. (hereinafter Krishnaswamy).

With respect to claim 8, although Levine discloses obtaining the profile data from a buffer (see column 11, lines 42-53), Levine does not expressly disclose setting one or more conditions for obtaining captured profile data when the memory buffer in the profile buffer is not fully allocated, and setting one or more conditions for transferring captured profile data from a first level in the profile buffer to a second level in the profile buffer.

However, Krishnaswamy discloses storing profile data in a buffer and reading the data from the buffer by setting an interrupt condition after a certain number of events, i.e. obtaining the data when the buffer is not fully allocated, for the purpose of sampling the profile data nonintrusively without significantly degrading performance (see column 6, lines 21-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to set a condition for obtaining the profile data of Levine when the buffer is not fully allocated, for the purpose of sampling the profile data nonintrusively without significantly degrading performance, as taught by Krishnaswamy.

Levine further discloses a memory hierarchy having two cache levels, in order balance cost and performance (see column 6, line 61 to column 7, line 8, which shows that the first level is faster but more costly than the second level). It is well known in the art that data is transferred between the cache levels in such memory hierarchies.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the buffer of Levine with two levels, and to transfer profile data from the first level to the second level given one or more set conditions, for the purpose of creating a hierarchy that balances cost and performance.

With respect to claim 9, the combination of Levine and Krishnaswamy further discloses receiving an interrupt or special event handler if the buffer that is assigned for the microarchitecture event is fully allocated or if a condition for obtaining captured profile data when the memory buffer in the profile buffer is not fully allocated is met (see Krishnaswamy, column 6, lines 21-45, which shows receiving an interrupt for obtaining the profile data from the buffer when the event-counting condition is met).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an interrupt for obtaining the profile data of Levine from the buffer, for the purpose of sampling the profile data nonintrusively without significantly degrading performance, as taught by Krishnaswamy.

With respect to claim 18, see the reasoning set forth above for claim 8. The operations recited by claim 18 are analogous to the method steps recited by claim 8.

With respect to claim 19, see the reasoning set forth above for claim 9. The operations recited by claim 19 are analogous to the method steps recited by claim 9.

With respect to claim 28, although Levine discloses obtaining the profile data from a buffer (see column 11, lines 42-53), Levine does not expressly disclose the limitation wherein

the hardware assisted dynamic optimizer sets one or more conditions for obtaining captured profiles from the profile buffer.

However, Krishnaswamy discloses storing profile data in a buffer and reading the data from the buffer by setting an interrupt condition after a certain number of events, for the purpose of sampling the profile data nonintrusively without significantly degrading performance (see column 6, lines 21-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to set a condition for obtaining the profile data of Levine when a condition is set, for the purpose of sampling the profile data nonintrusively without significantly degrading performance, as taught by Krishnaswamy.

With respect to claim 29, the combination of Levine and Krishnaswamy further discloses the limitation wherein a memory buffer in the second level of the profile buffer is assigned to a microarchitecture event, and wherein the hardware assisted dynamic optimizer accesses the profiles of the microarchitecture event when the memory buffer assigned to the microarchitecture event is fully allocated or when a condition for obtaining captured profiles is met (see Levine, column 11, lines 42-53, which shows that the buffer is of a predetermined size and is used in a round-robin fashion, and is therefore fully allocated when the profile data is obtained before being overwritten).

With respect to claim 30, the combination of Levine and Krishnaswamy further discloses the limitation wherein the hardware assisted dynamic optimizer accesses the profiles of a

microarchitecture event upon receiving an interrupt or special event handler (see Krishnaswamy, column 6, lines 21-45, which shows obtaining the profile data upon receiving an interrupt).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an interrupt for obtaining the profile data of Levine, for the purpose of sampling the profile data nonintrusively without significantly degrading performance, as taught by Krishnaswamy.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Pat. No. 5,915,114 to McKee et al. discloses a dynamic, trace-driven optimizer. U.S. Pat. App. Pub. No. 2002/00073406 to Gove discloses compiler optimization based on performance counter profiling.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (703) 305-0352. The examiner can normally be reached on Monday through Friday from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY

Michael J. Yigdall
Examiner
Art Unit 2122

mjy
April 2, 2004

TUAN DAM
SUPERVISORY PATENT EXAMINER